AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) An off-chip driver circuit, comprising;

a plurality of delay circuits, at least two of which have different delay times, in which the delay circuits receive a data signal and generate delayed data signals, respectively; and

a plurality of off-chip drivers for respectively receiving the delayed data signals from the respective delay circuits and generating respective output signals in response to respective control signals,

~~whrerein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals.~~

wherein the total number of the off-chip drivers to be activated at the same time is changed by the respective control signals which are generated in response to a desired drivability, and the activated off-chip drivers sequentially generate the output signals in response to the delay times, thereby increasing a total drivability of the off-chip driver circuit.

2. (currently amended) The off-chip driver circuit as claimed in claim 1, ~~wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.~~

wherein the off-chip driver comprises:

a first inverter for inverting the control signal;

a second inverter for inverting an output of the first inverter; and

an NAND gate for outputting the output signal in response to the delayed data signal and an output of the second inverter.

3. (currently amended) An off-chip driver circuit, comprising;

a plurality of off-chip drivers for respectively receiving a data signal and generating a plurality of output signals, respectively, in response to respective control signals; and

a plurality of delay circuits at least two of which have different delay times with respect to each other, in which the delay circuits respectively receive the output signals and generate delayed output signals, respectively,

~~whrerein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals.~~

wherein the total number of the off-chip drivers to be activated at the same time is changed by the respective control signals which are generated in response to a desired drivability, and the delay circuits sequentially generate the delayed output signals in response to the delay times, thereby increasing a total drivability of the off-chip driver circuit.

4. (currently amended) The off-chip driver circuit as claimed in claim 3, ~~wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.~~

wherein the off-chip driver comprises:

a first inverter for inverting the control signal;

a second inverter for inverting an output of the first inverter; and

an NAND gate for outputting the output signal in response to the data signal and an output of the second inverter.

5. (Canceled)

6. (currently amended) A data output circuit, comprising:

a plurality of delay circuits, at least two of which have different delay times with respect to each other, in which the delay circuits receive a data signal and generate delayed data signals, respectively;

a plurality of off-chip drivers for respectively receiving the delayed data signals from the respective delay circuits and generating respective output signals in response to respective control signals;

a pre-driver circuit adapted to receive the data signal and drive an output driver circuit; and

the output driver circuit connected to the output terminals of the off-chip drivers and the pre-driver circuit,

~~wherein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals, and total drivability of the data output circuit depends on the number of the off-chip drivers to be operated according to the control signals.~~

wherein the total number of the off-chip drivers to be activated at the same time is changed by the respective control signals which are generated in response to a desired drivability, and the activated off-chip drivers sequentially generate the output signals in response to the delay times, thereby increasing a total drivability of the off-chip drivers.

7. (previously presented) The data output circuit as claimed in claim 6, wherein the pre-driver circuit receives the data signal and performs a pull-up or a pull-down function according to a logical status of the data signal.

8. (currently amended) The data output circuit as claimed in claim 6, ~~wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.~~

wherein the off-chip driver comprises:

a first inverter for inverting the control signal;

a second inverter for inverting an output of the first inverter; and

an NAND gate for outputting the output signal in response to the delayed data signal and an output of the second inverter.

9. (previously presented) The data output circuit as claimed in claim 6, wherein the output driver circuit comprises output drivers connected to output terminals of the respective off-chip drivers and the pre driver circuit, wherein when the control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver is driven.

10. (currently amended) The data output circuit as claimed in claim 6, wherein ~~a~~ the total drivability of the off-chip drivers is 80% of a target drivability and a drivability of the pre driver circuit is 60% of the target drivability so that a drivability of the data output circuit varies from 60% of the target drivability to 140% of the target drivability.

11. (currently amended) A data output circuit, comprising:

a plurality of off-chip drivers for respectively receiving a data signal and generating a plurality of output signals, respectively, in response to respective control signals;

a plurality of delay circuits at least two of which have different delay times, in which the delay circuits respectively receive the output signals and generate delayed output signals, respectively;

a pre-driver circuit receiving the data signal and driving an output driver circuit; and

the output driver circuit connected to the output terminals of the delay circuits and the pre-driver circuit,

~~whrerein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals, and a total drivability of the data output circuit depends on the number of the off-chip drivers to be operated according to the control signals.~~

wherein the total number of the off-chip drivers to be activated at the same time is changed by the respective control signals which are generated in response to a desired drivability, and the delay circuits sequentially generate the delayed output signals in response to the delay times, thereby a total drivability of the off-chip drivers.

12. (previously presented) The data output circuit as claimed in claim 11, wherein the pre-driver circuit receives the data signal and performs a pull-up or a pull-down function according to the logical status of the data signal.

13. (currently amended) The data output circuit as claimed in claim 11, ~~wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being~~

~~low, the off-chip drivers perform NOR operations.~~

wherein the off-chip driver comprises:

a first inverter for inverting the control signal;

a second inverter for inverting an output of the first inverter; and

an NAND gate for outputting the output signal in response to the data signal and an output of the second inverter.

14. (previously presented) The data output circuit as claimed in claim 11, wherein the output driver circuit comprises output drivers connected to output terminals of the delay circuits and the pre driver circuit respectively, wherein when the control signal of a given off-chip driver is at an enable level, the output driver connected to the given off-chip driver is driven.

15. (currently amended) The data output circuit as claimed in claim 11, wherein ~~a~~ the total drivability of the off-chip drivers is 80% of a target drivability and a drivability of the pre driver circuit is 60% of the target drivability so that a drivability of the data output circuit varies from 60% of the target drivability to 140% of the target drivability.

16. (New) The off-chip driver circuit as claimed in claim 1, wherein the off-chip driver comprises:

an inverter for inverting the control signal; and

an NOR gate for outputting the output signal in response to the delayed data signal and an output of the inverter.

17. (New) The off-chip driver circuit as claimed in claim 3, wherein the off-chip driver comprises:

an inverter for inverting the control signal; and

an NOR gate for outputting the output signal in response to the data signal and an output of the inverter.

18. (New) The off-chip driver circuit as claimed in claim 6, wherein the off-chip driver comprises:

an inverter for inverting the control signal; and

an NOR gate for outputting the output signal in response to the delayed data signal and an output of the inverter.

19. (New) The off-chip driver circuit as claimed in claim 11, wherein the off-chip driver comprises:

an inverter for inverting the control signal; and

an NOR gate for outputting the output signal in response to the data signal and an output of the inverter.